IN THE CLAIMS

1. (Currently Amended) A computer processor, the processor comprising:

(a) a decode unit for decoding a stream of instruction packets from a memory, each instruction packet comprising a plurality of instructions;

(b) a first processing channel comprising a plurality of functional units and operable to perform control processing operations;

(c) a second processing channel comprising a plurality of functional units and operable to perform data processing operations;

wherein the decode unit is operable to receive an instruction packet and to detect if the instruction packet defines (i) at least two ~~a plurality of~~ control instructions or (ii) a plurality of instructions one or more of which is a data processing instruction, and wherein when the decode unit detects that the instruction packet comprises at least two ~~a plurality of~~ control instructions said control instructions are supplied to the first processing channel for execution in program order.

2. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect an instruction packet comprising three control instructions and control the control process to execute each of the three control instructions in the order in which they appear in the instruction packet.

3. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect an instruction packet containing a plurality of control instructions of equal length.

4. (Original) A computer processor according to claim 3, wherein the decode unit is operable to detect within an instruction packet a control instruction of a bit length between 18 and 24 bits.

5. (Original) A computer processor according to claim 4, wherein the decode unit is operable to detect within an instruction packet a plurality of control instructions each having a bit length of 21 bits.

6. (Original) A computer processor according to claim 1, wherein the decode unit is operable to receive and decode instruction packets of a bit length of 64 bits.

7. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect when there is at least one data processing instruction in the instruction packet and, in response thereto, to cause relevant data to be supplied to the data processing channel.

8. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect that the instruction packet comprises at least one data processing instruction and a further instruction selected from one or more of: a memory access instruction; a control instruction; and a data processing instruction.

9. (Original) A computer processor according to claim 8 wherein, at least one data processing instruction and said further instruction are executed simultaneously.

10. (Original) A computer processor according to claim 1, wherein the second processing channel is dedicated to the performance of data processing operations and data processing instructions are provided in assembly language.

11. (Original) A computer processor according to claim 1, wherein the control processing operations are performed on operands up to a first predetermined bit width and the data processing operations are performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width.

12. (Original) A computer processor according to claim 1, wherein the first processing channel comprises units selected from one or more of: a control register file; a control execution unit; a branch execution unit and a load/store unit.

13. (Original) A computer processor according to claim 1, wherein the second processing channel comprises a data execution path including a configurable data execution unit.

14. (Original) A computer processor according to claim 1, wherein the second processing channel comprises a data execution path including a fixed data execution unit.

15. (Original) A computer processor according to claim 13, wherein, in use, the configurable data execution unit operates according to single instruction multiple data principles.

16. (Original) A computer processor according to claim 14, wherein, in use, the fixed data execution unit operates according to single instruction multiple data principles.

17. (Original) A computer processor according to claim 1, wherein the data processing channel comprises one or more of a data register file and a load/store unit.

18. (Original) A computer processor according to claim 1, wherein a single load/store unit is accessed by both the control processing channel and the data processing channel through respective ports.

19. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect an instruction packet comprising at least one data processing instruction, wherein the bit length of the at least one data processing instruction is between 30 and 38 bits.

20. (Original) A computer processor according to claim 19, wherein the decode unit is operable to detect an instruction packet comprising at least one data processing instruction, wherein a bit length of the at least one data processing instruction is 34 bits.

21. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect an instruction packet comprising a data processing operation and a memory access instruction.

22. (Original) A computer processor according to claim 21, wherein the bit length of said memory access instruction is 28 bits.

23. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect an instruction packet comprising a data processing instruction and a control processing instruction.

24. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect a control processing instruction in C code or variant thereof.

25. (Original) A computer processor according to claim 1, wherein the decode unit is operable to detect a data processing instruction in assembly language.

26. (Currently Amended) A method of operating a computer processor which comprises first and second processing channels, each having a plurality of functional units, wherein the first processing channel is capable of performing control processing operations and the second processing channel is capable of performing data processing operations, the method comprising:

(a) receiving a sequence of instruction packets from a memory, each of said instruction packets comprising a plurality of instructions defining operations;

(b) decoding each instruction packet in turn by determining if the instruction packet defines:

(i) at least two ~~a plurality of~~ control instructions; or

(ii) at least one data processing instruction, and

wherein when the decode unit detects that the instruction packet comprises at least two ~~a plurality of~~ control instructions supplying said at least two ~~plurality of~~ control instructions to said first processing channel for execution in sequence.

27. (Previously Presented) A computer program product comprising a computer readable medium bearing a program code, which when processed by a computer, causes the computer to be operated according to the method of claim 26.

28. (Previously Presented) A computer readable medium bearing a program code, comprising a sequence of instructions for causing a computer to be operated according to the method of claim 26.

29. (Currently Amended) A computer readable medium bearing an instruction set for a computer including a first class of instruction packets each comprising two or more ~~a plurality of~~ control instructions for execution sequentially and a second class of instruction packets each comprising at least a data processing instruction and a further instruction for execution contemporaneously, said further instruction being selected from one or more of: a memory access instruction; a control instruction; and a data processing instruction.